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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/916,306	07/30/2001	Jun Koyama	12732-059001	8263

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EXAMINER	
EISEN, ALEXANDER	
ART UNIT	**PAPER NUMBER**
2674	

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/916,306	KOYAMA, JUN	
	Examiner	Art Unit	
	Alexander Eisen	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-20 and 46-58* is/are allowed.

6)☒ Claim(s) *1-10,21-45,59 and 60* is/are rejected.

7)☒ Claim(s) *61* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/1/04; and #3*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01 November 2004 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 2, 4, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al., ("Okumura"), US 5,945,972 (reference of record) in view of Perner.

With respect to claim 1 Okumura discloses a liquid crystal display device having a plurality of pixels, wherein the plurality of pixels comprises a plurality of storage circuits (230a and 230b; FIGS. 6-9); a write-in storage circuit selection portion (inverter 231, transfer gates 232a and 233a, switch signal 261) connected to a selected one of the plurality of storage circuits (for example, when the switch signal 261 is low transfer gate 233a is ON and an image signal 275 is applied to the memory cell 230b; see col. 18, lines 7-42); a read storage circuit selection

portion (232b and 233b) electrically connected to a selected one of the plurality of storage circuits.

Okumura does not disclose that the plurality of pixels respectively comprise a write-in transistor electrically connected to the write-in storage circuit selection portion, a read transistor electrically connected to the read storage circuit selection portion and a liquid crystal element electrically connected to the read transistor. Perner teaches a liquid crystal display device having a plurality of pixels, wherein the plurality of pixels respectively include integrated memory cells within each pixel and having a write-in transistor 32 electrically connected to the write-in storage circuit selection portion 14; a read transistor (36 and 38) electrically connected to the read storage circuit selection portion 18 and 22; and a liquid crystal element 100 (FIG. 2; col. 5, line 67 - col. 6, line 17) electrically connected to the read transistor (36, 38). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to improve the memory cell arrangement of Okumura by adding to it the write-in transistor electrically connected to the write-in storage circuit selection portion and the read transistor electrically connected to the read storage circuit selection portion, as taught by Perner, because it would allow the independent writing and reading operations, which in turn enables slow input data rate to match a variety of host systems and minimize flickers and artifacts (see Perner, col. 5, lines 1-10).

As to claims 2 and 4, Okumura teaches using SRAM and DRAM memory (see FIGS. 8-9; col. 18, lines 22-42).

As to claim 4, Perner teaches using DRAM memory circuits in each pixel.

In regard to claims 9 and 10, Perner teaches a laptop (personal PC) computer using LCD display (col. 8, lines 35-47). Even though Perner does not specifically teach that the LCD can be also used in such devices as television, a portable terminal, a video camera or a head mount display it would have been known to one of ordinary skill in the art at the time when the invention was made that LCD devices are commonly used in a broad spectrum of electronic devices, including those mentioned above.

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura in view of Perner and further in view of Yamazaki (reference of record, IDS).

Okumura discloses a liquid crystal display device having a plurality of pixels, wherein the plurality of pixels comprises a plurality of storage circuits.

Perner teaches a liquid crystal display device having a plurality of pixels, wherein the plurality of pixels respectively include integrated memory cells within each pixel and having a write-in transistor; a read transistor; and a liquid crystal element electrically connected to the read transistor. None of the above discloses ferroelectric memory that can be used in the storage circuits. Yamazaki teaches a storage circuit for LCD employing ferroelectric type of memory. It would have been obvious to one of ordinary skill in the art at the time when the invention was made that the memory taught by Yamazaki can be applied for the storage devices of Okumura-Perner, because it would allow to provide a display capable of rewriting only specified pixels as taught by Yamazaki, resulting in saving power, and also realize "resume" function, which stores the image at turning power off and restores it upon turning power back on (Yamazaki; col. 5, lines 42-50).

5. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura in view of Perner and further in view of Fonash et al., ("Fonash"), US 5,945,866.

Okumura discloses a liquid crystal display device having a plurality of pixels, wherein the plurality of pixels comprises a plurality of storage circuits. Perner teaches a liquid crystal display device having a plurality of pixels, wherein the plurality of pixels respectively include integrated memory cells within each pixel and having a write-in transistor; a read transistor; and a liquid crystal element electrically connected to the read transistor. None of the above teaches that the storage circuits can be formed on a glass or a plastic substrate. Fonash teaches that the circuit of LCD can be made on either glass or plastic substrates (FIG.1; col. 1, lines 44-52). It would have been obvious to one of ordinary skill in the art at the time when the invention was made that either substrate, glass and plastic, as taught by Fonash, can be used for manufacturing the storage circuits of Okumura-Perner, which will be readily recognized by those of ordinary skilled in the art at the time of the invention as an alternative material choice for manufacturing, without bringing any unexpected result. It also should be pointed out that neither Fonash nor applicant show any criticality of the choice or advantage of using one type of a substrate over another.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura in view of Perner and further in view of Johnson, US 4,752,118.

Okumura discloses a liquid crystal display device having a plurality of pixels, wherein the plurality of pixels comprises a plurality of storage circuits. Perner teaches a liquid crystal display device having a plurality of pixels, wherein the plurality of pixels respectively include integrated memory cells within each pixel and having a write-in transistor; a read transistor; and

a liquid crystal element electrically connected to the read transistor. None of the above teaches that the components of LCD can be manufactured using stainless steel substrate. Johnson teaches that the semiconductor circuits, including those for LCD, can be made using stainless steel substrates. It would have been obvious to one of ordinary skill in the art at the time when the invention was made that any known type of a substrate, stainless steel substrate taught by Johnson including, can be used for manufacturing the memory circuit of liquid crystal display device of Okumura-Perner, and it would be readily recognized by those of ordinary skilled in the art as an alternative choice for manufacturing, without requiring unduly experimentation or bringing unexpected result.

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura in view of Perner and further in view of Kobayashi et al., ("Kobayashi"), US 4,432,610.

Okumura discloses a liquid crystal display device having a plurality of pixels, wherein the plurality of pixels comprises a plurality of storage circuits. Perner teaches a liquid crystal display device having a plurality of pixels, wherein the plurality of pixels respectively include integrated memory cells within each pixel and having a write-in transistor; a read transistor; and a liquid crystal element electrically connected to the read transistor. Okumura and Perner do not teach or suggest, individually or in combination, that the storage circuits are formed on monocrystalline wafer substrate. Kobayashi teaches that the memory circuit for LCD can be made on monocrystalline wafer substrate (col. 5, lines 13-21 and FIG. 4). It would have been obvious to one of ordinary skill in the art at the time when the invention was made that the teachings of Kobayashi will complement the teachings of Okumura and Perner by providing a

concrete realization of how the memory circuits for Okumura-Perner display can be manufactured using a monocrystalline wafer substrate.

Double Patenting

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

9. Claims 21-45 and 59-60 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 3-5, 8-13 of copending Application No. 09/912,596. Although the conflicting claims are not identical, they are not patentably distinct from each other because, even though claims 21 and 33 of the current application are directed to LCD pixel memory structure and claims 3 and 4 of copending application – to EL pixel memory structure, the corresponding structures and functionality of their elements are exactly the same, and it would have been obvious to one of ordinary skill in the art at the time when the invention was made that similar element composition and functionality can be applied to any type of known matrix type of a display, the memory structure being in fact independent from the display type. It should be noted that claims 8-13 of copending application have been cancelled by amendment and subject matter of these claims is currently

represented by dependent claims 24-30 and 33-45. Accordingly, claims 22 and 34 of the application correspond to claim 5, claims 23 and 35-36 to claim 6, claims 24 and 37 to claims 22-23, claims 25 and 38 to claims 25-26, claims 26 and 39 to claims 28-29, claims 27-30 and 40-43 to claims 31-32, claims 31-32 and 44-45 to claims 37-38, and claims 59-60 to claims 44-45 of copending application respectively.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Allowable Subject Matter

10. Claims 11-20 and 46-58 are allowed.

11. Allowance of claims 11-20 is necessitated by amendment to claim 11, particularly by adding limitations, whereby a liquid crystal display device having n x m storage circuits, n write-in transistors, and n read transistors, includes a feature, where each of the n read transistors control reading of m storage circuits and each of the n write-in transistors controls writing of m storage circuits (see Applicant's arguments on page 14).

12. The reasons for allowance of claims 46-57 above have been conveyed to the applicant in the previous Office action.

13. Claim 61 is objected to as being dependent from rejected basis claim 1, but would be allowable if rewritten in independent form including all the limitations of the basis claim and any intervening claims.

The reasons for indicating allowable subject matter in claim 61: none of the references, either individually or in combination, teach or fairly suggest a liquid crystal display device as being claimed in independent claim 1, and wherein the write-in storage circuit selection portion

is electrically connected between the write-in transistor and the selected one of the plurality of storage circuits, and where the read storage circuit selection portion is electrically connected between the selected one of the plurality of the storage circuits and the read transistor.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

14. Applicant's arguments with respect to claims 1-10 have been fully considered but they are not persuasive.

Particularly, with respect to claim 1, the Applicant argues that "Perner's control signals 14, 18 and 22 cannot correspond to the recited selector portions because they are not connected to a selected one of the storage circuits, as recited in claim 1" [sic]. The Examiner respectfully disagrees. The control signals 14, 18 and 22 are conducted to the gates of respective write-in transistors 32, read transistors 36 and 38, which in turn are connected to respective storage circuit selected by the transistors and therefore these control signals are in fact connected to "the selected one of the storage circuits", as claim 1 is required.

The Applicant further argues that Perner would not provide a motivation to modify Okumura, since read and write operations in the latter are already independent. The Examiner respectfully disagrees in that, because Perner provides an additional advantage of selecting particular memory circuit by using two transistors 36 and 38 in series, which allows reading time-sequentially the entire cell array, Id. Col. 3, ll. 23-30.

The Applicant also argues that none of the prior art applied in the rejection, teach or suggest the recited arrangement, in which a write-in storage circuit selection portion is electrically connected to a selected one of the storage circuits and a write-in transistor is electrically connected to the write-in storage circuit selection portion. In Perner FIG .1 represents a single storage cell 34, part of an array of cells in a single pixel, this storage cell is written into through write-in transistor 32, gate of which is connected to the storage circuit selector portion represented by lines 14, where the line is assigned to a particular cell by the word wwl[0:2] – a three-bit word addressing six (n=6) storage cell. As can be seen from the figure, the selector circuit is connected to the storage cell through the write-in transistor 34, and also the write-in transistor is connected to the storage selector circuit 14.

The rejection is maintained.

As to claims 21-45 and 59-60, no terminal disclaimer have been filed in response to the provisional obviousness-type double patenting rejection and therefore the rejection is maintained. Since the copending application 09/912,596 has been passed to issue, the terminal disclaimer or cancellation of claims would be required to overcome the double patenting rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Eisen whose telephone number is (703) 306-2988. The examiner can normally be reached on M-F (9:00-5:00).

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander Eisen
Primary Examiner
Art Unit 2674

18 January 2005